LF43168
Dual 8-Tap FIR Filter

FEATURES

- 66 MHz Data and Computation Rate
- Two Independent 8-Tap or Single 16-Tap FIR Filters
- 10-bit Data and Coefficient Inputs
- 32 Programmable Coefficient Sets
- Supports Interleaved Coefficient Sets
- User Programmable Decimation up to 16:1
- Maximum of 256 FIR Filter Taps, 16 x 16 2-D Kernels, or 10 x 20-bit Data and Coefficients
- Replaces Harris HSP43168
- Package Styles Available:
  - 84-pin Plastic LCC, J-Lead
  - 100-pin Plastic Quad Flatpack

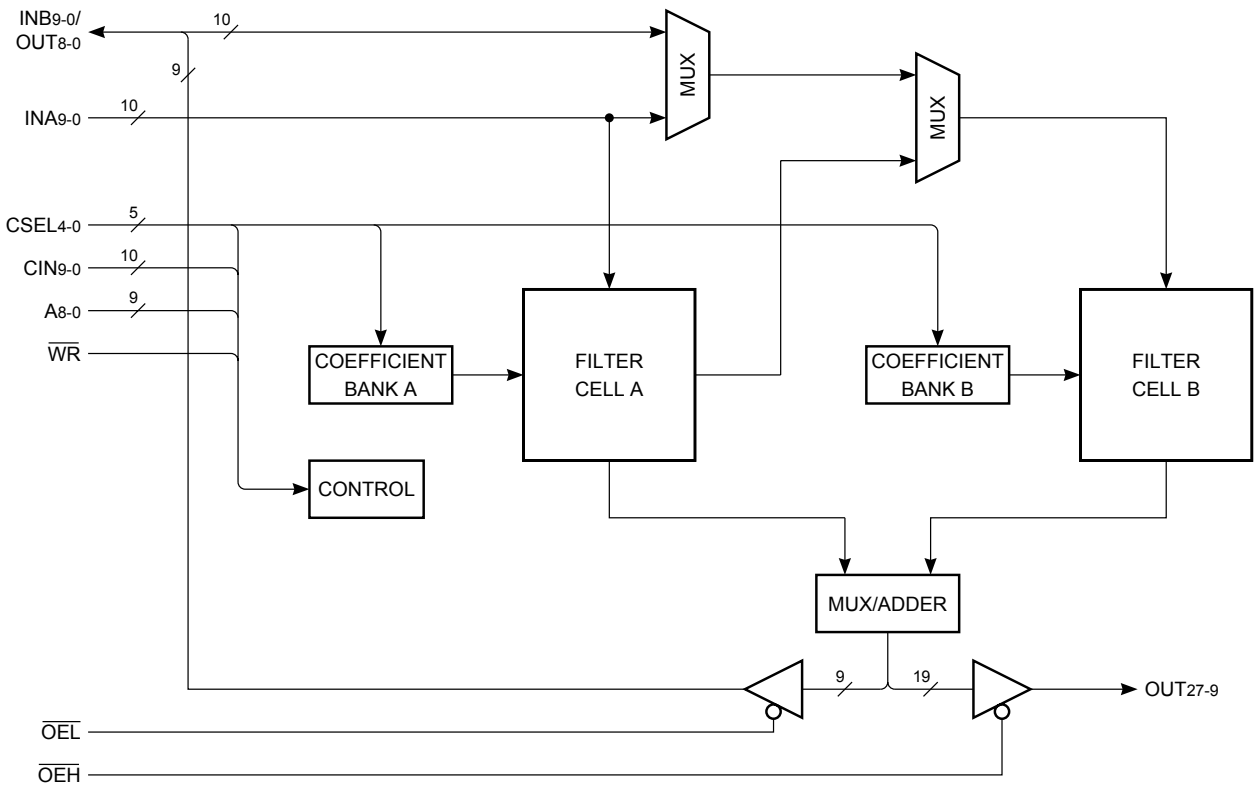
DESCRIPTION

The **LF43168** is a high-speed dual FIR filter capable of filtering data at real-time video rates. The device contains two FIR filters which may be used as two separate filters or cascaded to form one filter. The input and coefficient data are both 10-bits and can be in unsigned, two's complement, or mixed mode format.

The filter architecture is optimized for symmetric coefficient sets. When symmetric coefficient sets are used, each filter can be configured as an 8-tap FIR filter. If the two filters are cascaded, a 16-tap FIR filter can be implemented. When asymmetric coefficient sets are used, each filter is configured as a 4-tap FIR filter. If both filters are cascaded, an 8-tap filter can be implemented. The LF43168 can decimate the output data by as much as 16:1. When the device is programmed to decimate, the number of clock cycles available to calculate filter taps increases. When configured for 16:1 decimation, each filter can be configured as a 128-tap FIR filter (if symmetric coefficient sets are used). By cascading these two filters, the device can be configured as a 256-tap FIR filter.

There is on-chip storage for 32 different sets of coefficients. Each set consists of eight coefficients. Access to more than one coefficient set facilitates adaptive filtering operations. The 28-bit filter output can be rounded from 8 to 19 bits.

LF43168 BLOCK DIAGRAM



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature ..... –65°C to +150°C
Operating ambient temperature ..... –55°C to +125°C
VCC supply voltage with respect to ground ..... –0.5 V to +7.0 V
Input signal with respect to ground ..... –0.5 V to VCC + 0.5 V
Signal applied to high impedance output ..... –0.5 V to VCC + 0.5 V
Output current into low outputs ..... 25 mA
Latchup current ..... > 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	**Temperature Range** (Ambient)	**Supply Voltage**
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ **V**CC ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ **V**CC ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions (Note 4)*

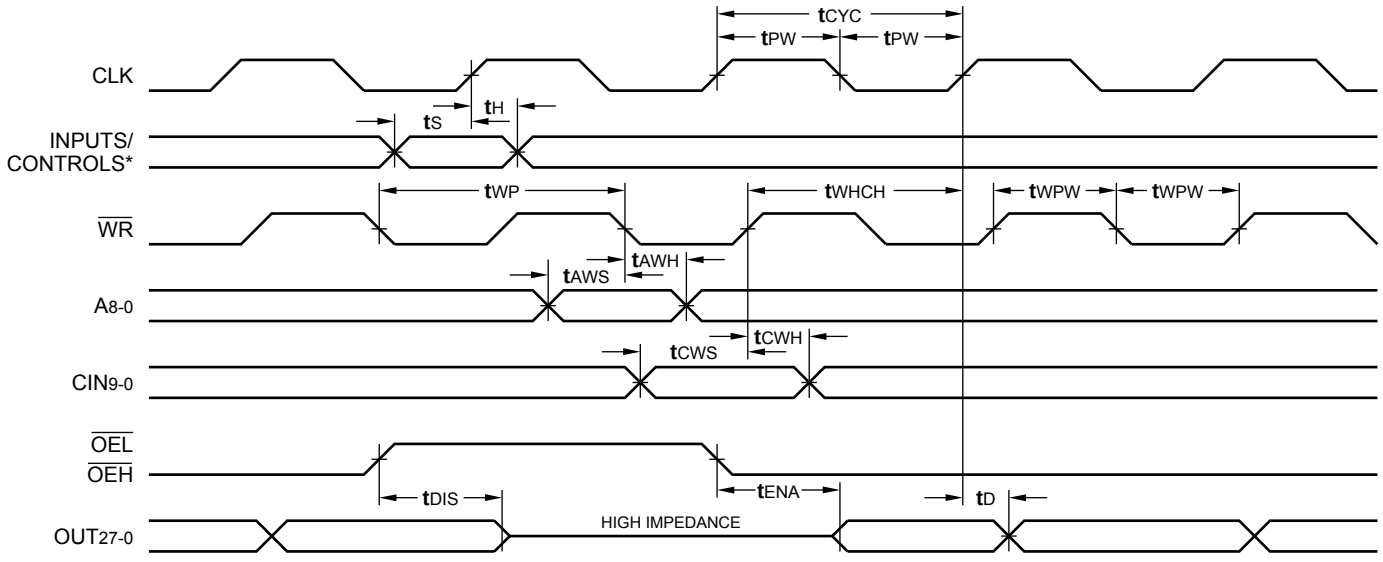
Symbol	**Parameter**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
VOH	Output High Voltage	**V**CC = Min., **I**OH = –2.0 mA	2.6			V
VOL	Output Low Voltage	**V**CC = Min., **I**OL = 4.0 mA			0.4	V
VIH	Input High Voltage		2.0		**V**CC	V
VIL	Input Low Voltage	(Note 3)	0.0		0.8	V
IIX	Input Current	Ground ≤ **V**IN ≤ **V**CC (Note 12)			±10	µA
IOZ	Output Leakage Current	Ground ≤ **V**OUT ≤ **V**CC (Note 12)			±10	µA
ICC1	**V**CC Current, Dynamic	(Notes 5, 6)			300	mA
ICC2	**V**CC Current, Quiescent	(Note 7)			500	µA
CIN	Input Capacitance	**T**A = 25°C, f = 1 MHz			12	pF
COUT	Output Capacitance	**T**A = 25°C, f = 1 MHz			12	pF

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE *Notes 9, 10 (ns)*

		LF43168–					
		30		22		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	30		22		15	
t_{PW}	Clock Pulse Width	12		8		7	
t_S	Input Setup Time	15		12		5	
t_H	Input Hold Time	0		0		0	
t_{WP}	Write Period	30		22		15	
t_{WPW}	Write Pulse Width	12		10		7	
t_{WHCH}	Write High to Clock High	5		3		2	
t_{CWS}	CIN_{9-0} Setup Time	12		10		5	
t_{CWH}	CIN_{9-0} Hold Time	0		0		0	
t_{AWS}	Address Setup Time	10		8		5	
t_{AWH}	Address Hold Time	0		0		0	
t_D	Output Delay		14		12		11
t_{ENA}	Three-State Output Enable Delay (Note 11)		12		12		12
t_{DIS}	Three-State Output Disable Delay (Note 11)		12		12		12

SWITCHING WAVEFORMS



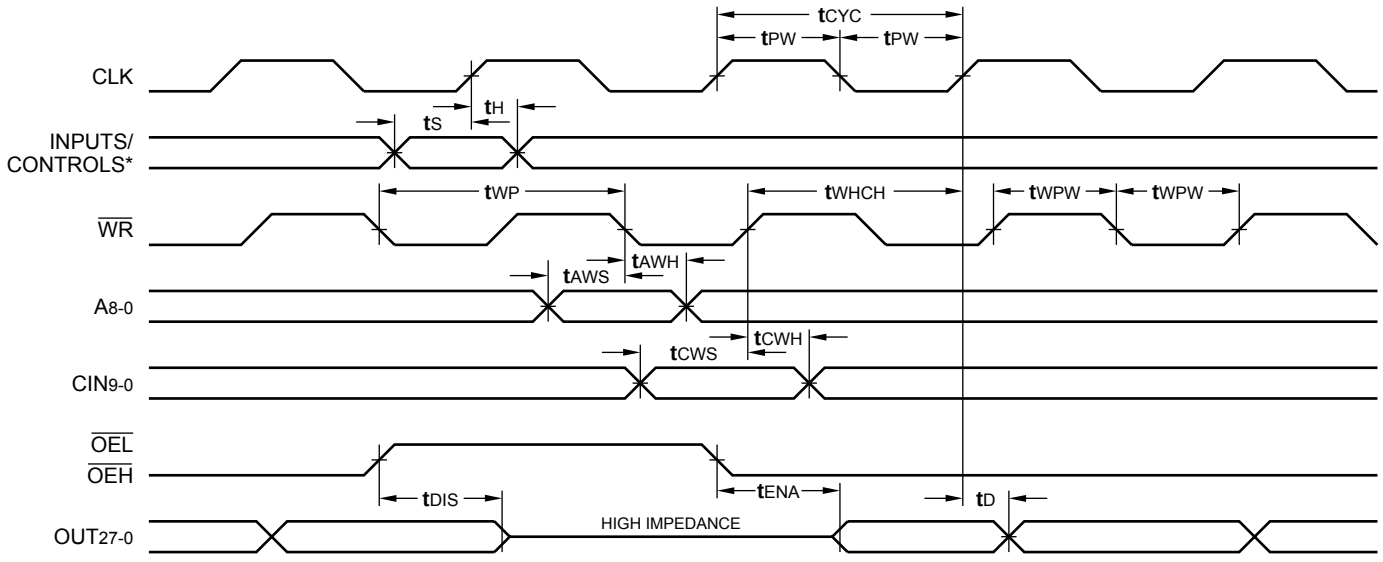
*includes INA_{9-0}, INB_{9-0}, $CSEL_{4-0}$, ACCEN, MUX_{1-0}, $\overline{SHFTEN}$, $\overline{FWRD}$, $\overline{RVRS}$, and $\overline{TXFR}$.

SWITCHING CHARACTERISTICS

MILITARY OPERATING RANGE *Notes 9, 10 (ns)*

		LF43168–					
		39*		30*		22*	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	39		30		22	
t_{PW}	Clock Pulse Width	15		12		8	
t_S	Input Setup Time	17		15		12	
t_H	Input Hold Time	0		0		0	
t_{WP}	Write Period	39		30		22	
t_{WPW}	Write Pulse Width	15		12		10	
t_{WHCH}	Write High to Clock High	8		5		3	
t_{CWS}	CIN_{9-0} Setup Time	15		12		10	
t_{CWH}	CIN_{9-0} Hold Time	0		0		0	
t_{AWS}	Address Setup Time	10		10		8	
t_{AWH}	Address Hold Time	0		0		0	
t_D	Output Delay		17		15		12
t_{ENA}	Three-State Output Enable Delay (Note 11)		12		12		12
t_{DIS}	Three-State Output Disable Delay (Note 11)		12		12		12

SWITCHING WAVEFORMS



*includes INA_{9-0}, INB_{9-0}, $CSEL_{4-0}$, ACCEN, MUX_{1-0}, $\overline{SHFTEN}$, $\overline{FWRD}$, $\overline{RVRS}$, and $\overline{TXFR}$.

***DISCONTINUED SPEED GRADE**

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above **V**CC will be clamped beginning at –0.6 V and **V**CC + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 20 MHz clock rate.

7. Tested with all inputs within 0.1 V of **V**CC or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except **t**DIS test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified **I**OH and **I**OL at an output voltage of **V**OH min and **V**OL max respectively. Alternatively, a diode bridge with upper and lower current sources of **I**OH and **I**OL respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on / turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between **V**CC and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device **V**CC and the tester common, and device ground and tester common.

b. Ground and **V**CC supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and **V**CC noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the **t**ENA test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the **t**DIS test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, VTH, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

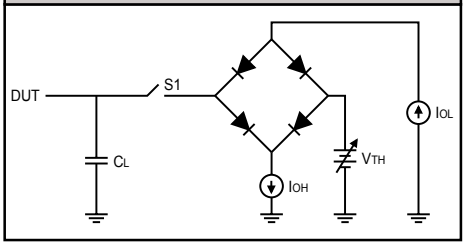


FIGURE B. THRESHOLD LEVELS