LF3320
Horizontal Digital Image Filter

FEATURES

- 83 MHz Data Rate
- 12-bit Data or Coefficients (Expandable to 24-bit)
- 32-Tap FIR Filter, Cascadable for More Filter Taps
- Over 49 K-bits of on-board Memory
- LF Interface™ Allows All 256 Coefficient Sets to be Updated Within Vertical Blanking
- Various Operating Modes: Dual Filter, Single Filter, Double Wide Data or Coefficient, Matrix Multiplication, and Accumulator Access.
- Selectable 16-bit Data Output with User-Defined Rounding and Limiting
- Supports Interleaved Data Streams
- Supports Decimation up to 16:1 for Increasing Number of Filter Taps
- 3.3 Volt Supply
- 144 Lead PQFP

DESCRIPTION

The **LF3320** filters digital images in the horizontal dimension at real-time video rates. The input and coefficient data are both 12 bits and in two's complement format. The output is also in two's complement format and may be rounded to 16 bits.

The LF3320 is designed to take advantage of symmetric coefficient sets. When symmetric coefficient sets are used, the device can be configured as a single 32-tap FIR filter or as two separate 16-tap FIR filters.

When asymmetric coefficient sets are used, the device can be configured as a single 16-tap FIR filter or as two separate 8-tap FIR filters. Multiple LF3320s can be cascaded to create larger filters.

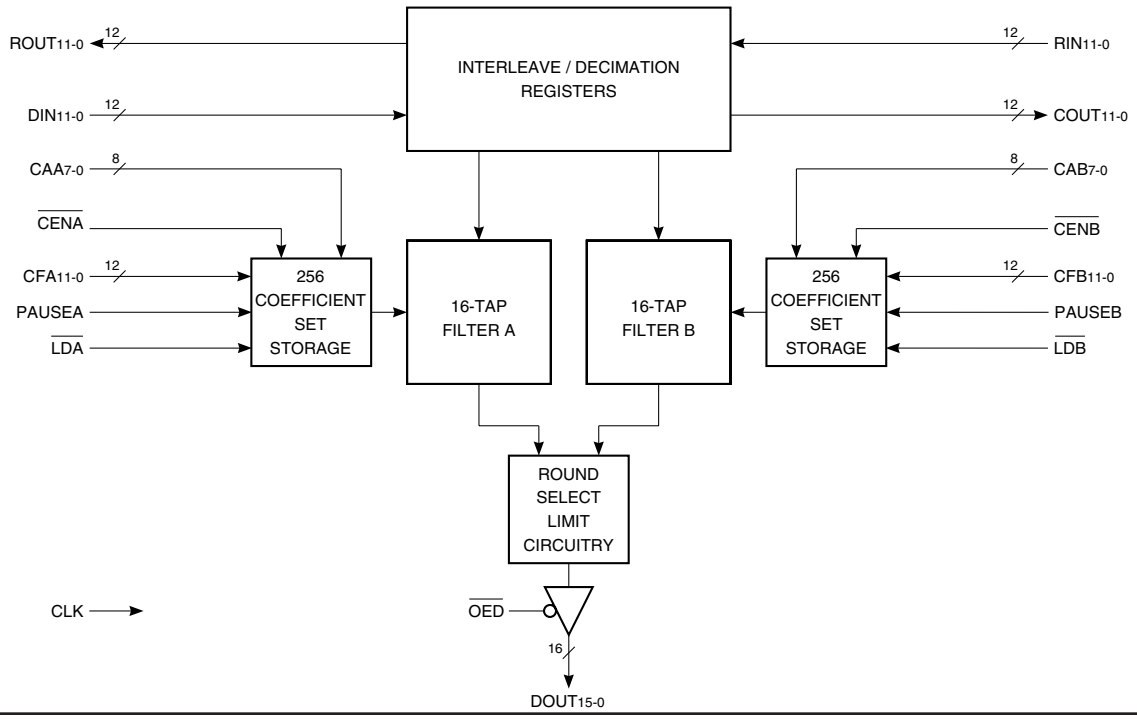
Interleave/Decimation Registers (I/D Registers) allow interleaved data to be fed directly into the device and filtered without separating the data into individual data streams.

The LF3320 can handle a maximum of sixteen data sets interleaved together. The I/D Registers and on-chip accumulators facilitate using decimation to increase the number of filter taps. Decimation of up to 16:1 is supported.

The LF3320 contains enough on-board memory to store 256 coefficient sets. Two separate LF Interfaces™ allow all 256 coefficient sets to be updated within vertical blanking.

NOTE: loading registers via the LF interface must not exceed 90MHz. The PAUSE pin must be used to throttle back the LF interface at clock speeds above 90MHz.

LF3320 BLOCK DIAGRAM



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
VCC supply voltage with respect to ground	–0.5V to +4.5V
Input signal with respect to ground	–0.5V to 5.5 V
Signal applied to high impedance output	–0.5V to 5.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA
ESD Classification (MIL-STD-883E METHOD 3015.7)	Class 3

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	3.00V ≤ **V**CC ≤ 3.60V
Active Operation, Military	–55°C to +125°C	3.00V ≤ **V**CC ≤ 3.60V

Electrical Characteristics *Over Operating Conditions (Note 4)*

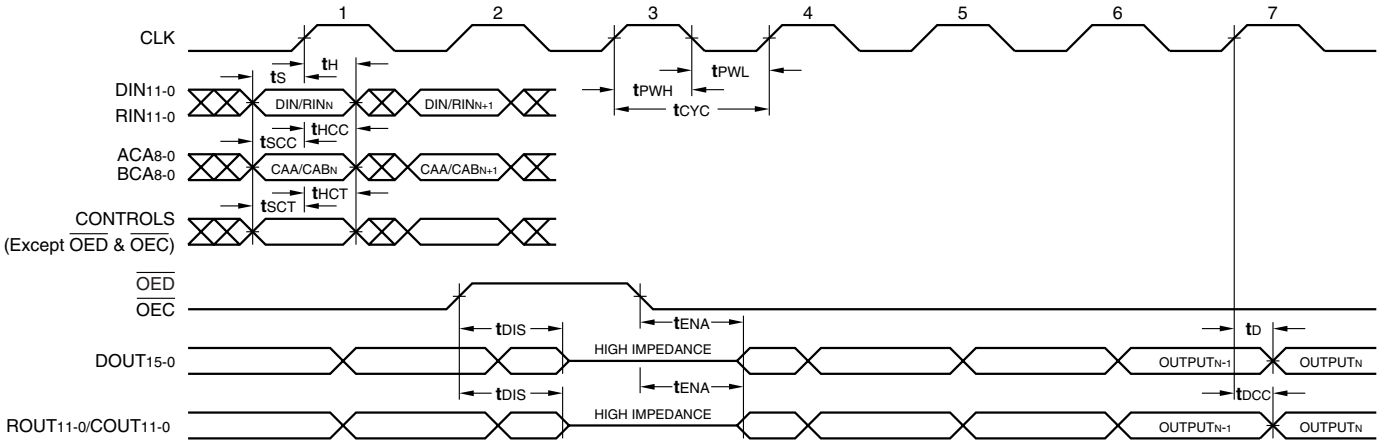
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VOH	Output High Voltage	**V**CC = Min., **I**OH = –4 mA	2.4			V
VOL	Output Low Voltage	**V**CC = Min., **I**OL = 8.0 mA			0.4	V
VIH	Input High Voltage		2.0		5.5	V
VIL	Input Low Voltage	(Note 3)	0.0		0.8	V
IIX	Input Current	Ground ≤ **V**IN ≤ **V**CC (Note 12)			±10	µA
IOZ	Output Leakage Current	Ground ≤ **V**OUT ≤ **V**CC (Note 12)			±10	µA
ICC1	**V**CC Current, Dynamic	(Notes 5, 6)			200	mA
ICC2	**V**CC Current, Quiescent	(Note 7)			2	mA
CIN	Input Capacitance	**T**A = 25°C, f = 1 MHz			10	pF
COUT	Output Capacitance	**T**A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF3320–							
		25		15		12		9	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	25		15		12		9	
t_{PWL}	Clock Pulse Width Low	10		7		5		5	
t_{PWH}	Clock Pulse Width High	10		7		5		5	
t_S	Input Setup Time	8		5		4		4	
t_H	Input Hold Time	0		0		0		0	
t_{SCT}	Setup Time Control Inputs	8		5		4		4	
t_{HCT}	Hold Time Control Inputs	0		0		0		0	
t_{SCC}	Setup Time Coefficient Control Input	8		5		4		4	
t_{HCC}	Hold Time Coefficient Control Input	0		0		0		0	
t_D	Output Delay		13		9		7		7
t_{DCC}	Cascade Output Delay		13		9		7.5		7.5
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		12		10		10
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		12		10		10

SWITCHING WAVEFORMS: DATA I/O

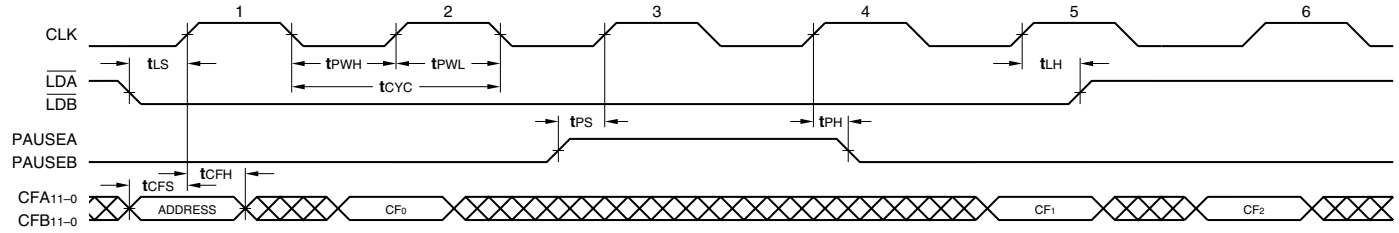


*DISCONTINUED SPEED GRADE

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LF3320– 25 Min	25 Max	15 Min	15 Max	12 Min	12 Max	9 Min	9 Max
t_{CFS}	Coefficient Input Setup Time	8		6		5.5			5.5
t_{CFH}	Coefficient Input Hold Time	0		0		0			0
t_{LS}	Load Setup Time	8		6		4			4
t_{LH}	Load Hold Time	0		0		0			0
t_{PS}	PAUSE Setup Time	8		5		4			4
t_{PH}	PAUSE Hold Time	0		0		0			0

SWITCHING WAVEFORMS: LF INTERFACE™



*DISCONTINUED SPEED GRADE

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. The device can withstand indefinite operation with inputs or outputs in the range of –0.5 V to +5.5 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with outputs changing every cycle and no load, at a 40 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages on a test fixture should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.0 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

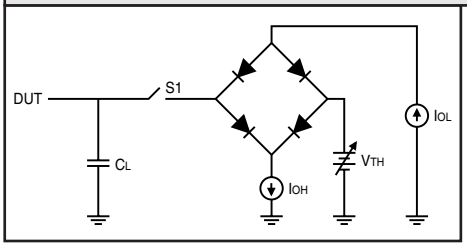


FIGURE B. THRESHOLD LEVELS